ELECTROSTATIC DISSIPATIVE STAGE AND EFFECTORS FOR USE IN FORMING LCD PRODUCTS

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] The following disclosure is a non-provisional application which claims priority to U.S. Provisional Application No. 60/911,817 filed Apr. 13, 2007, entitled "Electrostatic Dissipative Stage for Use in Forming LCD Products" and having named inventors Oh-Hun Kwon, Steve D. Hartline, Xiaofeng Tang, and Qiang Zhao, which application is incorporated by reference herein in its entirety.

BACKGROUND

[0002] 1. Field of the Disclosure

[0003] This disclosure is directed to stages and effectors for holding and manipulating glass substrates, and is particularly directed to processes for forming LCD displays utilizing such stages and effectors.

[0004] 2. Description of the Related Art

[0005] The manufacture of liquid crystal displays (LCDs) has becoming increasingly daunting as the industry continues to demand displays having improved features, such as greater size, better resolution, brighter colors, greater contrast, improved viewing angles, and longer viewing lives. Because of these demands, the industry has been required to improve the components and processes for forming the components within the LCDs. Notably, the industry has had to achieve the creation of thin film transistors (TFTs) and particularly arrays of thin film transistors that rival those of the semiconductor industry in forming integrated circuitry.

[0006] The formation of thin film transistors is an exacting process requiring creation of nanometer-sized films that are deposited in particular locations on a glass substrate. Ultimately, the series of deposited layers work together to form an array of transistors that facilitate controlling individual pixels on the screen and thus helping to deliver the image to the viewer. However, as it is well known, the formation of such TFT arrays is a highly technical endeavor requiring state of the art processing operations such as the formation or removal of nanometer-sized films in a controlled environment. Notably, a major concern of formation of a TFT array includes process induced damage such as for example, contamination. Because the process is so demanding, the current industry production efficiency for producing LCD panels is between 70% and 80%.

[0007] Accordingly, the industry continues to demand improved articles and processes for forming LCD panels that will improve the production efficiency, throughput, and the quality of the LCD panels formed.

SUMMARY

[0008] According to one aspect a process for producing a liquid crystal display (LCD) is disclosed which includes placing a glass substrate on a stage, and subjecting the glass substrate to at least one processing operation of a plurality of processing operations for forming an array of electronic devices on the glass substrate. The stage being electrostatic discharge (ESD) dissipative and having a surface portion that has a volume resistivity (R_v) within a range between about 1E5 Ωcm and about 1E11 Ωcm; and

[0009] According to another aspect, a LCD stage is disclosed which includes a body comprising a surface portion, the surface portion being an electrostatic discharge (ESD) dissipative material having a volume resistivity (R_v) within a range between about 1E5 Ωcm and about 1E11 Ωcm.

[0010] According to another aspect, a LCD glass substrate effector is disclosed that includes a body comprising an arm portion extending from the body, wherein the body has a surface portion being an electrostatic discharge (ESD) dissipative material having a volume resistivity (R_v) within a range between about 1E5 Ωcm and about 1E11 Ωcm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The present disclosure may be better understood, and its numerous features and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0012] FIG. **1**A includes an illustration of a cross-sectional view of a workpiece including a portion of a glass substrate and a stage in preparation for forming a TFT array on the glass substrate according to one embodiment.

[0013] FIG. **1**B is a cross-sectional view of the workpiece illustrated in FIG. **1**A after forming electrodes according to one embodiment.

[0014] FIG. **1**C is a cross-sectional view of the workpiece illustrated in FIG. **1**B after forming a dielectric layer according to one embodiment.

[0015] FIG. **1**D is a cross-sectional view of the workpiece illustrated in FIG. **1**C after forming an intermediate semiconductive layer portion according to one embodiment.

[0016] FIG. **1**E is a cross-sectional view of the workpiece illustrated in FIG. **1**D after forming a top semiconductive layer portion according to one embodiment.

[0017] FIG. **1**F is a cross-sectional view of the workpiece illustrated in FIG. **1**E after forming a transparent electrode layer portion according to one embodiment.

[0018] FIG. **1**G is a cross-sectional view of the workpiece illustrated in FIG. **1**E after forming source/drain layer portions according to one embodiment.

[0019] FIG. **1**H is a cross-sectional view of the workpiece illustrated in FIG. **1**G after forming a passivation layer portion according to one embodiment.

[0020] FIG. **2** is a cross-sectional diagram of a portion of a LCD panel according to one embodiment.

[0021] FIG. **3** is a cross-sectional diagram of a portion of a stage of effector according to one embodiment.

[0022] FIG. **4** is a cross-sectional diagram of a portion of a stage or effector according to one embodiment.

[0023] FIG. **5** is a top view of a stage having a patterned working surface according to one embodiment.

[0024] FIG. **6** is a cross-sectional view of a portion of a stage having raised portions defining a working surface according to one embodiment.

[0025] FIG. **7** is a perspective view of a LCD glass substrate effector in accordance with one embodiment.

[0026] FIG. **8** is a plot of volume resistivity measured at an applied voltage of 1V for 17 samples in accordance with an embodiment.

[0027] FIG. **9** is a plot of volume resistivity measured at an applied voltage of 10 V for 17 samples in accordance with an embodiment.

[0028] FIG. **10** is a plot of volume resistivity measured at an applied voltage of 100 V for 17 samples in accordance with an embodiment.